

TONY GLADVIN GEORGE

Bangalore, India

Mobile: +91-9632500136, E-Mail: ewizlab@gmail.com

In quest of assignments in the areas of FPGA/ DSP on Wireless/Video domain.

Executive Synopsis

- ⌘ A judicious professional with **over 4 years'** experience in modelling, development, and optimization of DSP CODECs on FPGA& DSP in India & Singapore.
- ⌘ Currently associated with **Mahindra Satyam Ltd., as Senior Software Engineer.**
- ⌘ Experience in 802.16e WIMAX Wireless Standard and H.264 Video Standard.
- ⌘ Quality exposure in managerial activities entailing technical leadership & guidance to the team members, planning, scheduling tasks, holding discussions with clients for design-related changes & implementation, project progress monitoring and delivery as per quality, time and budgetary norms.
- ⌘ Resourceful and deft in all phases of the SDLC (Requirement analysis, development, testing and troubleshooting), with strong understanding of Software Engineering Process.
- ⌘ Holds several IEEE papers published in DSP Processing Applications.
- ⌘ An effective communicator with honed relationship management, analytical, logical and problem-solving abilities.

Education

- M.Tech. VLSI(Very Large Scale Integration) from SRM Institute of Science & Technology, 76% in 2005.
- B.E. Electronics and Communication from Periyar University, 74% in 2003.

Feathers in the Cap

- "Extra Mile Award" for the achievements in CODEC development from Tata Elxsi Ltd. in 2007.
- "Appreciation Award" for the achievements in DSP development from Satyam Computer Services Ltd. in 2005.
- "Young Scientist Award" for the achievements in Biomedical Image Processing from VM Research Foundation University in 2003.
- Reviewer of esteemed "IEEE Transactions Industrial Electronics".

Skill Set

Technical Skills

Domain Knowledge	:	Wireless CODEC, Video CODEC
Processor	:	TI DSP, ARM9E
FPGA	:	Xilinx, Altera
Languages	:	C, Verilog, VHDL
Development Tools	:	Code Composer Studio, Model Sim, VC++
Research Tools	:	MATLAB

Managerial

- Handling pre-sales activities including negotiation of service contract & timeframe required for the commencement & completion of each activity.
- Providing consultancy on Project Planning, Execution and Management in tune with the core business objectives (including risk management, effort / time / cost estimation, and contingency planning).
- Implementing project plans within pre-set budgets and deadlines.
- Monitoring project progress as per scheduled deadlines for various tasks and taking necessary steps to ensure completion within time, cost and effort parameters.

Functional

- Interfacing with clients for business gathering, conducting system analysis and finalising technical / functional specifications and high level design documents for the project.
- Contributing to the design, development, testing, troubleshooting and debugging of the software.
- Ensuring smooth implementation and testing at client location.
- Interacting with clients to understand and accommodate changes in the design.
- Providing post-implementation, application maintenance and enhancement support to the client with regard to the product / software application.

Experience Details

Since Mar'08 with Mahindra Satyam Ltd., as Senior Engineer
(NYSE: SAY. India's leading engineering services outsourcing vendor)

Key Projects Handled

- **Video codec on Wireless codec SoC** Duration: Since Apr'09
Role: R&D Engineer
Team Size: 15
Technical Environment: C, Verilog, VC++, Matlab
Scope: The project involves design and implementation of Wimax (802.16e) PHY Layer Encoder & Decoder for Mobile station and H.264 Video Codec on SOC platform consisting of TI DSP (TMS320C64x) & FPGA (Xilinx Vertex 4).
Responsibilities:
 - ✓ Define the system architecture for H.264 Video transmission through Wimax on SoC platform.
 - Software Hardware partitioning
 - Develop C code targeted for TMS320C64x
 - Develop RTL, Timing closure, optimization for Xilinx.

- **Wimax Physical layer (Singapore)** Duration: Mar'08 to Apr'09
Role: R&D Engineer
Team Size: 25
Technical Environment: Verilog, C, Modelsim, Xilinx ISE, Matlab
Scope: The project encompasses the design and implementation of Wimax (802.16e) PHY Layer (Baseband) Encoder and Decoder for Mobile station in SOC with FPGA & TMS320C5510.
Responsibilities:
 - ✓ Defining system architecture for Wimax.
 - ✓ Handling the development of:
 - Simulation model, C code and RTL code for Xilinx
 - LDPC-error correction codes,
 - channel estimation/ equalisation,
 - Timing Synchronization and
 - Ranging module.
 - Define test cases for modules.
 - Timing closure, Algorithm Optimisation, Area Optimisation

Jun'06 to Mar'08 with Tata Elxsi Ltd., Bangalore as Senior Engineer
(The Product Design arm of the USD 22 Billion Tata Group)

Key Projects Handled

- **JPEG2000 Codec Hardware for Japanese Client** Duration: Aug'07 to Mar'08
Role: Project Lead
Team Size: 8
Technical Environment: C, Verilog HDL, VC++6, NC-Sim
Keywords: JPEG2000, JPEG 2K, Area Optimisation, Frequency Optimisation, Wavelet, Lossless, Lossy
Scope: The project entailed the design and implementation of JPEG2000 Encoder and Decoder in 90nm ASIC. JPEG 2000 is a wavelet-based image compression standard, and it gains up to about 20% compression performance for medium compression rates in comparison to the first JPEG standard.
Responsibilities:
 - ✓ Leading the design and documentation of efficient hardware architecture for real time operation of the CODEC. Developing RTL in Verilog HDL.
 - ✓ Involved in the development of test plans and unit integration.

- **H.264 Codec Hardware for Japanese Client** Duration: Dec'06 to Aug'07
Role: Project Lead
Team Size: 10
Technical Environment: C, Verilog HDL, VC++ 6, Modelsim
Keywords: H.264, AVC, Advanced Video Coding, Intra, Inter, Frame, Entropy, CAVLC, CABAC
Scope: The project entailed the design and implementation of H.264 High Profile Encoder and Decoder in SOC, as a standard for video compression, for a Japanese video equipment manufacturing giant.
Responsibilities:
 - ✓ Handling onsite interaction with the client for requirement gathering and architecture suggestions.
 - ✓ Studying H.264 CODEC and modularisation of the functions for porting onto hardware.
 - ✓ Designing efficient hardware architecture for real time operation of the CODEC by parallelism and pipelining.
 - ✓ Developing the RTL in Verilog HDL.Contributions: Successfully handled deputation to Japan for the specification phase.

- **CAVLC Decoder on FPGA-StratixII for Japanese Client** Duration: Jun'06 to Nov'06
Role: Configuration Controller & Developer
Team Size: 5
Technical Environment: C, Verilog HDL, VC++6, Modelsim, Quartus, StratixII FPGA

Scope: The project entailed porting CAVLD (VLC decoding module of H.264 decoder) on to StratixII FPGA. Context-adaptive variable-length coding (CAVLC) is a form of entropy coding used in H.264/ MPEG-4 AVC video encoding, and is an inherently lossless compression technique. In H.264/MPEG-4 AVC, it is used to encode residual, zig-zag order, and blocks of transform coefficients.

Responsibilities:

- ✓ Studying TEL H.264 decoder C source code and preparing design document, targeting the hardware.
- ✓ Modifying the design document for achieving higher speed by parallelism and pipelining.
- ✓ Handling the development of the design in Verilog HDL.
- ✓ Optimising hardware of CAVLD module using Static Timing Analysis (STA).
- ✓ Preparing CM plan (Configuration Management) and setting up VSS (Visual Source Safe) Server for the same.
- ✓ Tracking all the codes and important documents for future reference.

Contributions: Overcame several challenges inherent in the project by maintaining seamless communication with the client. Met all deadlines, which helped the client to deploy the product in time.

May'05 to Jun'06 with Satyam Computer Services Ltd., Bangalore as Software Engineer

(Leading name in the IT industry)

Key Projects Handled

- **H.264 and MP3 Porting on OMAP ARM9 for Taiwanese Client** Duration: May'05 to Jun'06
Team Size: 4 Role: Team Member
Technical Environment: C, OMAP CCS

Selected List of Papers Published

- "The Architecture of Fast H.264 CAVLC Decoder and its FPGA Implementation", Tony Gladvin George at el, Presented at IEEE Conference ITHMSP-2007, International Workshop on Intelligent Information Hiding and Multimedia Signal Processing, Kaohsiung, Taiwan, November 26-28, 2007.
- "A New Fast Architecture for HD H.264 CAVLC multi-syntax Decoder and its FPGA Implementation", Tony Gladvin George at el, Presented at IEEE Conference ICCIMA07, International Conference on Computational Intelligence and Multimedia Applications 2007, Mepco Schlenk Engineering College, Sivakasi, December 13-15, 2007.
- Tony Gladvin George, Malmurugan. N, Shaan Geo, "Rapid prototyping of Floating point code for fixed point Processors." Presented at International Conference ICMM2006, Universiti Malaya, Malaysia during 14, Mar 2006.
- Tony Gladvin George, Malmurugan. N, "Mammographic Enhancement Algorithm using Wavelet Transform with Donoho's denoising threshold" - Presented at International Conference on Matlab and Simulink, Bangalore, 29 September 2005.
- Tony Gladvin George, Malmurugan. N, Nagappan A., Z C Alex, V Krishnaveni, "Mammographic Enhancement Algorithm using Balanced Multiwavelet Transform for detection of Microcalcifications" - Presented at International Conference ICIS2005, Universiti Teknologi Petronos, Malaysia during 1-3 December 2005.
- Tony Gladvin George, Malmurugan. N, Danie T. John, "Watershed processing in cDNA Microarray" Presented at National Conference NACCA2006, Kovilpetti, during 2, March 2006.
- Tony Gladvin George, Malmurugan. N. "Early detection of Microcalcifications in Mammogram using wavelet filter banks" Presented at CIT, Tumkur, during April 2005.

Personal Snippets

Date of Birth	:	10/08/1980
Passport Details	:	F4420409 (Issued at Cochin. Valid up to 21/08/2015)
Address	:	Chirayath House, P.O. Potta-680 722 (Kerala, India)
References	:	To be provided upon request